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APPELLANTS:	Ho-Rang JANG	CONF. NO.:	6847
SERIAL NO.:	10/759,270	GROUP:	2185
FILED:	January 20, 2004	EXAMINER:	Jae Un Yu
FOR:	CACHE MEMORY DEVICE AND METHOD OF CONTROLLING THE CACHE MEMORY DEVICE		

REVISED APPELLANTS' BRIEF ON APPEAL UNDER 37 C.F.R. §41.37

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TABLE OF CONTENTS

Page

Sir:

In accordance with the provisions of 37 C.F.R. §41.37, Appellants submit the following:

I. REAL PARTY IN INTEREST:

The real party in interest is Samsung Electronics Co., Ltd.

II. RELATED APPEALS AND INTERFERENCES

None

III. STATUS OF CLAIMS:

1. Claims 1-26 are pending. Claims 1-4, 10, 11, 13, 17-19, 22, 23, 25 and 26 have been rejected. Claims 5-9, 12-16, 20-21 and 24 are objected to.

2. Claims 1-4, 17-19, 22 and 23 stand rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent Application No. 2001/0032297 (Morikawa et al.) in view of U.S. Patent Application No. 2004/0221138 (Rosner et al.).

3. Claims 10, 11, 13 and 25 stand rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent Application No. 2001/0032297 (Morikawa et al.) in view of U.S. Patent Application No.

2004/0221138 (Rosner et al.) in further view of US Patent No. 6,505,253 (Chiu et al.).

Claims 1-4, 10, 11, 13, 17-19, 22, 23, 25 and 26 are appealed.

IV. STATUS OF AMENDMENTS:

No amendment to the claims has been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER:

The following explains the subject matter set forth in each independent claim and each dependent claim argued separately referring to the specification by page and line number, and to the drawings, by reference characters in accordance with 37 C.F.R. § 41.37(c)(1)(v). Namely, a concise explanation of the subject matter set forth in each of independent claims 1, 10, 17 and 22, and dependent claims 2-4, 11, 13, 18, 19, 23, 25 and 26 is set forth below.

a. INDEPENDENT CLAIMS

Claim 1

Claim 1 is directed a cache memory device for a digital signal processor (DSP). See e.g., FIGS. 3 and 4.

Claim 1 recites:

> a first cache memory for enabling a running flag signal in response to a given interrupt signal from a DSP core of the DSP to provide a given number of first instructions to the DSP core, and for disabling the running flag signal

As illustrated in FIGS. 3 and 8 and as disclosed on page 6, lines 3-11 of the present specification, a digital signal processor (DSP) core 10 may send an interrupt signal INT_ACK to a first interface unit 110. The first interface unit 110 may transmit the interrupt signal INT_ACK to a first cache memory 120. Page 6, lines 12-22. Page 7, lines 4-19 of the present specification further disclose that "[w]hen first cache memory 120 receives the interrupt signal INT_ACK, the first cache memory 120 enables a running flag signal RUN_F[,]" and "the first cache memory 120 outputs the first instructions INS_RE1." Finally, page 7, lines 26-32 of the present specification disclose "the first cache memory 120 ceases operations and disables the running flag signal RUN_F."

Claim 1 further recites:

> a second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled.

As illustrated in FIGS. 3 and 8 and as disclosed on page 6, lines 23-31 of the present specification, a second memory cache may provide a second instruction INS_RE2 to the DSP core 10. Page 7, lines 33-34 and

page 8, lines 1-17 of the present specification also disclose that the second cache memory 130 may operate when the running flag signal RUN_F is disabled.

Claim 10

Claim 10 is directed to a method of controlling a cache memory device in a digital signal processor (DSP). See e.g., FIGS. 3 and 6.

Claim 10 recites:

> (a) first providing an instruction to a DSP core of the DSP from a cache memory, in response to a request from the DSP core

As illustrated in FIGS. 3 and 8 and as disclosed on page 6, lines 3-11 of the present specification, a digital signal processor (DSP) core may send an interrupt signal INT_ACK to a first interface unit 110. The first interface unit 110 may transmit the interrupt signal INT_ACK to a second cache memory 130. Page 6, lines 23-31 of the present specification disclose that the second cache memory 130 may provide a second instruction INS_RE2 to the DSP core 10.

Claim 10 also recites:

> (b) enabling a running flag signal in another cache memory in response to an interrupt signal received thereto from the DSP core

Page 7, lines 4-19 of the present specification further disclose that "[w]hen first cache memory 120 receives the interrupt signal INT_ACK, the first cache memory 120 enables a running flag signal RUN_F."

Claim 10 further recites:

> (c) second providing, in response to a request from the DSP core, a given number of instructions from the another cache memory to the DSP core that are different from the first provided instruction

Page 6, lines 23-31 of the present specification disclose that the first instruction INS_RE1 may instruct the DSP core 10 to check an interrupt request state and read related input variables. Page 6, lines 23-31 of the present specification further disclose the second instruct INS_RE2 may instruct the DSP core 10 to execute regular program.

Claim 10 also recites:

> (d) disabling the running flag signal and ceasing said second providing step when the given number of instructions reaches a threshold value.

Page 7, lines 26-32 of the present specification disclose "the first cache memory 120 ceases operations and disables the running flag signal RUN_F" after reaching a threshold value.

Claim 17

Claim 17 relates to a cache memory device for a digital signal processor (DSP). See e.g., FIGS. 8, 9, 11 and 12.

Claim 17 recites:

> a first cache memory providing a first instruction in response to a program address received from a DSP core of the DSP, if there is no first instruction corresponding to the program address, and outputting a first miss signal

Page 16, lines 14-23 of the present specification disclose that a program address may be transmitted to first through third cache memories 220, 230, 240. Page 19, lines 23-33 and page 20, lines 1-2 of the present specification disclose that a first instruction INS_R1 from the first cache memory 220 may be sent to a DSP core 10. Page 19, lines 23-33 and page 20, lines 1-2 of the present specification also disclose that the first cache memory may output a miss signal MISS_L. See also page 7, lines 20-25 of the present specification.

Claim 17 also recites:

> a second cache memory providing at least one second instruction to the DSP core in response to a given interrupt signal and the first miss signal and, the second cache memory further disabling a running flag signal based after a given number of second instructions have been provided to the DSP core

Page 19, lines 23-33 and page 20, lines 1-2 of the present specification disclose that a second cache memory 230 may provide a

second instruction INS_R2 to the DSP core 10. Page 20, lines 3-12 of the present specification disclose and as illustrated in FIG. 11, the second cache memory 230 may provide the second instruction INS_R2 until it reaches a given value. Once the given value is reached, the second cache memory 230 may disable a running flag RUN_F.

Claim 17 further recites:

> a third cache memory which provides a third instruction to the DSP core in response to the first miss signal, when the running flag signal is disabled.

Page 20, lines 3-12 of the present specification disclose and as illustrated in FIG. 12, a third cache memory 240 may provide a third instruction INS_R3 when it receives a miss signal MISS_L and the running flag RUN_F may be disabled.

Claim 22

Claim 22 relates to a method of controlling a cache memory device in a digital signal processor (DSP). See, e.g., FIG. 8.

Claim 22 recites:

> (a) first providing a first instruction from a first cache memory to a DSP core in response to a program address from the DSP core

As illustrated in FIG. 8 and as disclosed on page 16, lines 14-23 of the present specification, a digital signal processor (DSP) core may send a program address PR_ADD to a first interface unit 110. The first interface unit 210 may transmit the program address PR_ADD to a first cache memory 220.

Claim 22 also recites:

> (b) second providing at least one second instruction from a second cache memory to the DSP core in response to the program address based on at least one of an output of a first miss signal from the first cache memory and an enabling of a running flag signal by the second cache memory

Page 17, lines 15-24 of the present specification disclose that the second cache memory may operate in response to a miss signal MISS_L from the first cache memory. Page 17, lines 15-24 also disclose that the second cache memory may enable the running flag signal RUN_F.

Claim 22 further recites:

> (c) disabling the running flag signal and ceasing step (b) when a number of second instructions provided to the DSP core reaches a given value

Page 17, lines 30-34 and page 18, lines 1-5 of the present specification disclose that the second cache memory stops operations and may disable the running flag signal RUN_F once a given number of second instructions INS_R2 has been sent to the core DSP.

Claim 22 also recites:

> (d) third providing a third instruction from a third cache memory to the DSP core in response to the program address based on at least one the first miss signal output from the first cache memory and a disabling of the running flag signal by the second cache memory

Page 18, lines 6-10 of the present specification disclose that a third cache memory may operate when the running flag signal RUN_F is disabled. The third cache memory may output the third instruction INS_R3.

Claim 22 recites:

> (e) enabling the running flag signal at the second cache memory when an interrupt signal is received thereto from the DSP core.

Page 72, lines 15-24 of the present specification disclose that the second cache memory may enable the running flag signal RUN_F.

B. DEPENDENT CLAIMS

Claim 2

Claim 2 recites the cache memory device of claim 1, further comprising:

> a first interface unit which interfaces the DSP core, first cache memory and second cache memory

FIGS. 3 and 8 illustrate a first interface unit 110, 210. Page 6, lines 3-11 of the present specification disclose that the first interface unit 110, 210 may receive program addresses PRO_ADD, interrupt signals INT_ACK, etc. from a DSP core 10 and transmit the program addresses PRO_ADD, interrupt signals INT_ACK, etc. to a first cache memory 120, 220 and a second cache memory 130, 230. The first interface unit 110, 210 may also receive instructions from the first cache memory 120, 220 and the second cache memory 130, 230 and transmit the instructions to the DSP core 10.

Claim 2 further recites:

> a second interface unit which interfaces the first cache memory, second cache memory and a program memory that stores instructions for the DSP core

Page 8, lines 18-30 of the present specification disclose that a second interface unit 140, 240 may interface with the first cache memory 120, 220 and the second cache memory 130, 230. The second interface unit 140, 240 may contain a memory 40 similar to the one illustrated in FIG. 1.

Claim 3

Claim 3 recites the cache memory device of claim 1, wherein:

> the given number of first instructions enable the DSP core to check a state of the interrupt request and to read relevant input variables.

Page 6, lines 23-31 of the present specification disclose that the first instruction INS_RE1 provided by the first cache memory 120 may be used to check an interrupt request state and read related input variables.

Claim 4

Claim 4 further recites the first cache memory of the cache memory device of claim 2.

Claim 4 recites:

> a cache memory block which stores a given one of the given number of first instructions received from the program memory in response to a corresponding write address and outputs each one of the given number of first instructions in response to a corresponding read address; and
>
> a cache controller which generates the write address, read address, and a prefetch address using a program address received from the DSP core via the first interface unit, wherein the cache controller transmits the prefetch address to the program memory via the second interface unit in order to receive a given first instruction.

FIG. 4 illustrates a detail block diagram of the first cache memory 120, and FIG. 5 details a cache memory block of FIG. 4.

Page 8, lines 31-34 and page 9, lines 1-8 of the present specification disclose that the cache memory block 150 may include storage registers 151 to store first instructions INS1 in response to write address WADD and output each one of the given number of first instructions in response to a

corresponding read address. See also page 13, lines 3-13 and page 14, lines 1-9 of the present specification.

Claim 11

Claim 11 recites the method of claim 10.

Claim 11 recites:

> (e) repeating steps (a) through (d) iteratively until there are no further instruction requests from the DSP core.

FIG. 6 illustrates a method of operating a cache memory device. Page 11, lines 22-28 of the present specification disclose that functions 2100 – 2600 (i.e., steps a - d) illustrated in FIG. 6 "may be repeated until the DSP core 10 request no further instructions."

Claim 13

Claim 13 recites the method of claim 10.

Claim 13 recites:

> (f) determining whether or not the given number of instructions in step (c) reaches the given value based on the accumulated count value.

Page 11, lines 22-28 and FIG. 6 disclose that at function 2500, the first cache memory 120 determines whether the given number of instructions have reached a given value.

Claim 18

Claim 18 recites the cache memory device of claim 17, further comprising:

> a first interface unit which interfaces the DSP core, first cache memory and second cache memory

FIGS. 3 and 8 illustrate a first interface unit 110, 210. Page 6, lines 3-11 of the present specification disclose that the first interface unit 110, 210 may receive program addresses PRO_ADD, interrupt signals INT_ACK, etc. from a DSP core 10 and transmit the program addresses PRO_ADD, interrupt signals INT_ACK, etc. to a first cache memory 120, 220 and a second cache memory 130, 230. The first interface unit 110, 210 may also receive instructions from the first cache memory 120, 220 and the second cache memory 130, 230 and transmit the instructions to the DSP core 10.

Claim 18 further recites:

> a second interface unit which interfaces the first cache memory, second cache memory and a program memory that stores instructions for the DSP core

Page 8, lines 18-30 of the present specification disclose that a second interface unit 140, 240 may interface with the first cache memory 120, 220 and the second cache memory 130, 230. The second interface unit 140, 240 may contain a memory 40 similar to the one illustrated in FIG. 1.

Claim 19

Claim 19 further recites the first cache memory of the cache memory device of claim 18.

Claim 19 recites:

> a cache memory block which stores a given one of the given number of first instructions received from the program memory in response to a corresponding write address and outputs each one of the given number of first instructions in response to a corresponding read address; and
>
> a cache controller which generates the write address, read address, and a prefetch address using a program address received from the DSP core via the first interface unit, wherein the cache controller transmits the prefetch address to the program memory via the second interface unit in order to receive a given first instruction.

FIG. 4 illustrates a detail block diagram of the first cache memory 120, and FIG. 5 details a cache memory block of FIG. 4.

Page 8, lines 31-34 and page 9, lines 1-8 of the present specification disclose that the cache memory block 150 may include storage registers 151 to store first instructions INS1 in response to write address WADD and output each one of the given number of first instructions in response to a corresponding read address. See also page 13, lines 3-13 and page 14, lines 1-9 of the present specification.

Claim 23

Claim 23 recites the method of claim 22.

Claim 23 recites:

> (f) iteratively repeating steps (a) through (e) until there are no further instruction requests from the DSP core.

FIG. 6 illustrates a method of operating a cache memory device. Page 11, lines 22-28 of the present specification disclose that functions 2100 – 2600 (i.e., steps a - e) illustrated in FIG. 6 "may be repeated until the DSP core 10 request no further instructions."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL:

Appellant seeks the Board's review of the following rejections:

1. Claims 1-4, 17-19, 22, 23 and 26 under 35 U.S.C. §103(a) over Morikawa et al. in view of Rosner et al; and
2. Claims 10, 11, 13 and 25 under 35 U.S.C. §103(a) over Morikawa et al. in view of Rosner et al. in further view of Chiu et al.

VII. ARGUMENTS:

Claims 1-4 rise and fall together.

Claims 10, 11, 13 and 25 rise and fall together.

Claims 17-19 rise and fall together.

Claims 22, 23 and 26 rise and fall together.

A. THE REJECTION OF CLAIMS 1-4, 17-19, 22, 23 AND 26 UNDER 35 U.S.C. 103(a) SHOULD BE WITHDRAWN BECAUSE EVEN ASSUMING *ARGUENDO* THAT MORIKAWA et al. COULD BE COMBINED WITH ROSNER et al. (WHICH APPELLANTS DO NOT ADMIT), THE RESULTANT COMBINATION STILL FAILS TO TEACH OR FAIRLY SUGGEST ALL FEATURES OF INDPENDENT CLAIMS 1, 17 AND 22

1. BRIEF DISCUSSION OF MORIKAWA ET AL.

Morikawa et al. teaches data processing system including a cache memory apparatus 5 and a lower-level memory 9. Morikawa et al. further teaches that the cache memory apparatus 5 includes a naked cache 6 and a miss-cache cache 7. Paragraph [0028].

In a control operation of the cache memory apparatus 5, a processor 1 sends a prefetch instruction or a load instruction to the cache memory apparatus 5. If the prefetch instruction or the load instruction produces a cache hit, i.e., the data is in the naked cache 6 or the miss-cache cache 7, the operation stops. Paragraphs [0034] and [0037]. On the other hand, if

there is a cache miss in both the naked cache 6 and the miss-cache cache 7, a data block is stored in the naked cache 6 from the lower-level memory 9. Paragraphs [0035] and [0037]. Morikawa et al. also teaches that the processor 1 sets a target flag 19 to "0" or "1" depending on whether the instruction is a prefetch instruction or a load instruction, respectively.

2. BRIEF DISCUSSION OF ROSNER ET AL.

Rosner et al. teaches multiple parallel processing in a computer system. Rosner et al. teaches a system 1 including a memory 105, a fetch unit 110, an apportion/tag unit 130, and multiple parallel processing units 105-153. Paragraph [0012].

Rosner et al. teaches that the memory 105 contains instructions to be processed. The fetch unit 110 retrieves those instructions from the memory 105. The fetch unit 110 further provides a single stream of instructions, which is then apportioned into segmented by the apportion/tag unit 130. The apportion/tag unit 130 may tag each of the segments to identify the next segment in the sequential order. The segments are distributed to parallel processing units 150-153 for processing according to the apportionment.

a. INDEPENDENT CLAIMS 1, 17 AND 22

The above rejection should be withdrawn because combination of Morikawa et al. and Rosner et al. fails to suggest or teach each and every limitation recited in independent claims 1, 17 and 22. A proper *prima facie* of obviousness of claims 1, 17 and 22 can only be established if each and every feature set forth in the claims are disclosed by a combination of Morikawa et al. and Rosner et al. *In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)*; M.P.E.P. § 2143.03.

Morikawa et al. and Rosner et al. fail to teach or fairly suggest a cache memory for enabling and disabling a running flag signal in response to an interrupt signal from a digital signal processor (DSP) as recited in claim 1 and 22, and similarly recited in claim 17. Because Morikawa et al. and Rosner et al. fails to teach or fairly suggest these features, the rejection should be withdrawn.

i. INDEPENDENT CLAIM 1

As discussed above, claim 1 recites a first cache memory for enabling and disabling a running flag in response to an interrupt signal from a digital signal processor (DSP). As it is well known to a person of ordinary skill in the art and as disclosed on page 7, lines 4-19 of the present specification, a running flag signal, when enabled indicates a state when

the cache memory may receive instructions in response to the interrupt request.

The Examiner alleges that an L2 cache 9 (first cache memory) enables and disables a target flag 19 (running flag signal). The Examiner further alleges that the target flag 19 is enabled when it is set to "0" and is disabled when it is set to "1." Page 2 of the Final Office Action dated January 25, 2007.

Morikawa et al. clearly teaches that "the processor 1 sets the target flag 19 to "0" via the control signal line 17" and that "the processor 1 sets the target flag 19 to "1" via the control signal 17." (Emphasis added). Paragraph [0035] and [0038]. Morikawa et al. also teaches that the processor 1 sets the target flag 19 to "0" if the "prefetch instruction produces a cache miss"; and, the processor 1 sets the target flag to "1" "if the load instruction produces a cache miss." Paragraph [0035] and [0038].

In response to Appellants' remarks filed on October 30, 2006, the Examiner alleges that the target flag is part of the first cache memory. Page 9 of the Final Office Action dated January 25, 2007. Appellants respectfully submit that the Examiner's interpretation of Morikawa et al. is incorrect, and the Examiner's response is a contradiction of his own rejection.

As remarked above, Morikawa et al. clearly teaches that the target flag 19 is set by the processor 1. Paragraph [0035] and [0038]. In

addition, on page 2 of the Final Office Action dated January 25, 2007, the Examiner alleges that an L2 cache is the first cache memory for enabling a running flag signal as recited in claim 1. In response to Appellants' remarks, the Examiner alleges "the examiner considers the 'target flag' (Paragraph 35) as a part of the 'first cache memory.'" Page 9 of the Final Office Action dated January 25, 2007. However, the Examiner alleged that **L2 cache 9** is the first cache memory, and paragraph [0035] and FIG. 2 of Morikawa et al. clearly shows the target flag 19 as part of **an L1 cache 5.** Therefore, at best, the target flag 19 is part of the cache-miss cache 7.

Claim 1 further recites that the running flag signal is enabled when the first cache memory receives an interrupt signal from the DSP. As remarked above, Morikawa et al. teaches that the processor 1 sets the target flag 19. Even if the target flag 19 is part of the first cache memory, Morikawa et al. clearly teaches that the target flag is set to "0" or "1" based on whether the prefetch instruction produces a cache miss or the load instruction produces a cache miss, respectively, by the processor 1.

For at least the reasons given above, Appellants submit that the combination of Morikawa et al. and Rosner et al. fails to teach or fairly suggest the features recited in claim 1.

ii. INDEPENDENT CLAIM 17

In rejecting independent claim 17, the Examiner applies the same logic applied to rejecting claim 1 with respect to Morikawa et al. and Rosner et al.

As discussed above with respect to the rejection of claim 1, Morikawa et al. clearly teaches that the target flag is set to "0" or "1" based on whether the prefetch instruction produces a cache miss or the load instruction produces a cache miss, respectively, by the processor 7. Paragraphs [0035] and [0038].

Claim 17 recites, *inter alia*:

> a second cache memory providing at least one second instruction to the DSP core in response to a given interrupt signal and the first miss signal and, the second cache memory further disabling a running flag signal based after a given number of second instructions have been provided to the DSP core (Emphasis added.)

As remarked above, Morikawa et al. teaches that the processor 1 sets the target flag 19 based on its own generated signal.

For at least the reasons given above, Appellants submit that the combination of Morikawa et al. and Rosner et al. fails to teach or fairly suggest the features recited in claim 17.

iii. INDEPENDENT CLAIM 22

In rejecting independent claim 22, the Examiner applies the same logic applied to rejecting claims 1 and 17 with respect to Morikawa et al. and Rosner et al.

As discussed above with respect to the rejection of claims 1 and 17, Morikawa et al. Morikawa et al. clearly teaches that the target flag is set to "0" or "1" based on whether the prefetch instruction produces a cache miss or the load instruction produces a cache miss, respectively, by the processor 7. Paragraphs [0035] and [0038].

Claim 22 recites, *inter alia*:

> (b) second providing at least one second instruction from a second cache memory to the DSP core in response to the program address based on at least one of an output of a first miss signal from the first cache memory and an enabling of a running flag signal by the second cache memory;
>
> (c) disabling the running flag signal and ceasing step (b) when a number of second instructions provided to the DSP core reaches a given value (Emphasis added.)

As remarked above, Morikawa et al. teaches that the processor 1 sets the target flag 19.

For at least the reasons given above, Appellants submit that the combination of Morikawa et al. and Rosner et al. fails to teach or fairly suggest the features recited in claim 22.

b. DEPENDENT CLAIMS 2-3, 18, 19, 23 AND 26

Dependent claims 2-3, dependent on claim 1; dependent claims 18 and 19 dependent on claim 17; dependent claims 23 and 26, dependent on claim 22, are also patentable for at least all the reasons stated above with respect to their respective base claim.

B. THE REJECTION OF CLAIMS 10, 11, 13 AND 25 UNDER 35 U.S.C. 103(a) SHOULD BE WITHDRAWN BECAUSE EVEN ASSUMING *ARGUENDO* THAT MORIKAWA et al. COULD BE COMBINED WITH ROSNER et al. IN FURTHER VIEW OF CHIU et al. (WHICH APPELLANTS DO NOT ADMIT), THE RESULTANT COMBINATION STILL FAILS TO TEACH OR FAIRLY SUGGEST ALL FEATURES OF INDEPENDENT CLAIM 10

1. A BRIEF DISCUSSION OF CHIU ET AL.

Chiu et al. teaches methods of controlling congestion in a computer network during multicast transmission. Chiu et al. further teaches establishing a multicast repair tree. A repair head station retransmitting a selected message received from a sender station to an affiliated group of member stations upon receipt from a member station of an information message (ACK/NACK message) indicating that said selected message was not received. Column 2, lines 58-67.

a. INDEPENDENT CLAIM 10

In rejecting claim 10, the Examiner applies the same logic applied to rejecting claims 1, 17 and 22 with respect to Morikawa et al. and Rosner et al. The Examiner further alleges that neither Morikawa et al. nor Rosner et al. teaches "ceasing said second providing step when the given number of instructions reaches a threshold value," but Chiu et al. teaches such feature.

First, claim 10 recites, *inter alia*:

> (d) disabling the running flag signal and ceasing said second providing step when the given number of instructions reaches a threshold value. (Emphasis added.)

Although in the Final Office Action, the Examiner alleges that Morikawa et al. teaches disabling the running flag signal, i.e., "[s]etting the 'target flag' to "0" [sic]. Page 10 of the Final Office Action dated January 25, 2007. For consistency, Appellants assume the Examiner meant that the target flag is set to "1." As remarked above, setting the target flag to "0" or "1" enables the naked cache memory 6 to store data from the lower-level memory 9 depending on whether there is a prefetch instruction miss or a load instruction miss. Paragraphs [0035] and [0038]. Nowhere in Morikawa et al. does it teach "disabling the running flag signal" "when the given number of instructions reaches a threshold level" as recited in claim 10.

In the remarks submitted on October 30, 2006, Appellants submitted that the Examiner allegations that the "Load Instruction" in step (c) is also equivalent to "a request from the DSP core" as well as the interrupt signal from (b) is incorrect. In response, the Examiner alleges, without any evidence or citation, that the "interrupt signal" is broader in scope than the term "load instruction." The Examiner further alleges that the interrupt signal is any signal that interrupts a system to perform certain tasks. Accordingly, the Examiner alleges that the "load instruction" interrupts a system to perform certain tasks. The Examiner's understanding of "load instruction" is simply incorrect.

With reference to FIG. 3 of Morikawa et al., at step 31 it is determined whether an instruction is a prefetch instruction. If the instruction is not a prefetch instruction, then it is determined that the instruction is a load instruction. Paragraph [0036]. If there is a cache hit, then at step 36, data is transferred from the naked cache memory 6 or cache-miss cache 7 to a resister 2 of the processor 1. Paragraph [0037]. If there is a cache miss, then data is transferred to the naked cache memory 6 from the lower-level memory 9. Paragraph [0038]. Accordingly, even if "interrupt signal" is broader in scope than the term "load instruction," nowhere in Morikawa et al. does it suggest or teach that the "load instruction" interrupts a system to perform certain tasks as alleged by the Examiner.

For at least the reasons given above, Appellants submit that the combination of Morikawa et al. and Rosner et al. fails to teach or fairly suggest the features recited in claim 10. Chiu et al. also fails to cure the deficiency of Morikawa et al. and Rosner et al. Accordingly, claim 10 is patentable over the Examiner's cited references.

2. DEPENDENT CLAIMS 11, 13 AND 25

Dependent claim 11, dependent on claim 10; dependent claim 13, dependent to claim 10; and dependent claim 25, dependent to claim 10, are also patentable for at least all the reasons stated above with respect to claim 10.

X. CONCLUSION:

In light of the foregoing arguments, Appellants respectfully request the Board to reverse the Examiner's rejection of claims 1-4, 10, 11, 13, 17-19, 22, 23, 25 and 26.

The Commissioner is authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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APPENDIX A – CLAIMS

Claims on Appeal:

1. A cache memory device for a digital signal processor (DSP), comprising:

a first cache memory for enabling a running flag signal in response to a given interrupt signal from a DSP core of the DSP to provide a given number of first instructions to the DSP core, and for disabling the running flag signal; and

a second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled.

2. The cache memory device of claim 1, further comprising:

a first interface unit which interfaces the DSP core, first cache memory and second cache memory; and

a second interface unit which interfaces the first cache memory, second cache memory and a program memory that stores instructions for the DSP core.

3. The cache memory device of claim 1, wherein the given number of first instructions enable the DSP core to check a state of the interrupt request and to read relevant input variables.

4. The cache memory device of claim 2, wherein the first cache memory includes:

a cache memory block which stores a given one of the given number of first instructions received from the program memory in response to a corresponding write address and outputs each one of the given number of first instructions in response to a corresponding read address; and

a cache controller which generates the write address, read address, and a prefetch address using a program address received from the DSP core via the first interface unit, wherein the cache controller transmits the prefetch address to the program memory via the second interface unit in order to receive a given first instruction.

5. The cache memory device of claim 4, wherein the cache controller further includes:

a first register which receives the program address from the first interface unit and outputs the program address as a request address;

a second register which, in response to the interrupt signal sets a first received program address as a start address;

a third register which generates the prefetch address based on the start address;

a first subtraction unit which subtracts the start address from the request address to output the read address to the cache memory block;

a second subtraction unit which subtracts the start address from the prefetch address to output the write address to the cache memory block;

a hit/miss determination unit which outputs a hit signal if the read address is determined as valid, and which otherwise outputs a miss signal;

a counter which counts a number of times the hit signal is output, accumulates the count value and outputs the accumulated count value; and

a control signal generator which determines whether or not the number of times the hit signal is output reaches a threshold value based on the accumulated count value and enables the running flag signal when the number of times the hit signal is output reaches the threshold value.

6. The cache memory device of claim 5, wherein

the third register generates the prefetch address when the hit signal is output from the hit/miss determination unit, and

the prefetch address includes a plurality of addresses that continuously increase in value from the start address.

7. The cache memory device of claim 5, wherein the counter is reset when another interrupt signal is received.

8. The cache memory device of claim 5, wherein

the hit/miss determination unit outputs the miss signal if the read address output from the first subtraction unit is outside a given address range of the cache memory block or if the first instruction corresponding to the read address is invalid,

the control signal generator outputs a given control signal in response to the miss signal, and

the second register resets the start address in response to the control signal.

9. The cache memory device of claim 8, wherein

the second register stores the program address used to generate the read address that is outside the given address range and sets the stored program address as a new start address in response to the control signal, and

the third register transmits the new start address to the program memory in response to the control signal.

10. A method of controlling a cache memory device in a digital signal processor (DSP), comprising:

(a) first providing an instruction to a DSP core of the DSP from a cache memory, in response to a request from the DSP core;

(b) enabling a running flag signal in another cache memory in response to an interrupt signal received thereto from the DSP core;

(c) second providing, in response to a request from the DSP core, a given number of instructions from the another cache memory to the DSP core that are different from the first provided instruction; and

(d) disabling the running flag signal and ceasing said second providing step when the given number of instructions reaches a threshold value.

11. The method of claim 10, further comprising:

(e) repeating steps (a) through (d) iteratively until there are no further instruction requests from the DSP core.

12. The method of claim 10, wherein step (c) further includes:

(c1) generating a read address in response to a received program address;

(c2) outputting a miss signal and resetting a start address if the read address is not within a given address range, or if one of the given number of instructions corresponding to the read address is invalid;

(c3) transmitting the reset start address in order to receive a write instruction;

(c4) generating a write address based on the reset start address and storing the write instruction;

(c5) outputting a hit signal and the write instruction if the read address is within the given address range, or if the given instruction corresponding to the read address is valid;

(c6) counting a number of times the hit signal is output;

(c7) outputting an accumulated count value; and

(c8) iteratively repeating steps (c1) through (c6) to provide the given number of instructions, until a count value of the counting in step (c6) reaches a given value.

13. The method of claim 10, further comprising:

(f) determining whether or not the given number of instructions in step (c) reaches the given value based on the accumulated count value.

14. The method of claim 12, wherein step (c1) further includes:

(c11) setting a first received one of a plurality of received program addresses as a start address; and

(c12) generating the read address by subtracting the start address from a request address that represents a plurality of consecutively received program addresses.

15. The method of claim 12, wherein

the start address reset in step (c2) is the program address corresponding to the read address for which the miss signal is output, and

step (c4) further includes generating the write address by subtracting the reset start address from the received program address.

16. The method of claim 12, wherein step (c5) further includes:

(c51) generating a prefetch address using the start address;

(c52) generating a write address by subtracting the start address from the prefetch address; and

(c53) storing the write instruction corresponding to the prefetch address.

17. A cache memory device for a digital signal processor (DSP), comprising:

a first cache memory providing a first instruction in response to a program address received from a DSP core of the DSP, if there is no first instruction corresponding to the program address, and outputting a first miss signal;

a second cache memory providing at least one second instruction to the DSP core in response to a given interrupt signal and the first miss signal and, the second cache memory further disabling a running flag

signal based after a given number of second instructions have been provided to the DSP core; and

a third cache memory which provides a third instruction to the DSP core in response to the first miss signal, when the running flag signal is disabled.

18. The cache memory device of claim 17, further comprising:

a first interface unit which interfaces the DSP core, first cache memory second cache memory and third cache memory; and

a second interface unit which interfaces the first cache memory, second cache memory, third cache memory and a program memory that stores instructions for the DSP core.

19. The cache memory device of claim 18, wherein the second cache memory includes:

a cache memory block which stores the second instructions, each second instruction received from the program memory in response to a corresponding write address, each second instruction output from the cache memory block in response to a corresponding read address; and

a cache controller which generates the write address, the read address, and a prefetch address using the program address received from

the DSP core via the first interface unit, the cache controller transmitting the prefetch address to the program memory via the second interface unit.

20. The cache memory device of claim 19, wherein the cache controller includes:

an input circuit which outputs the program address received in response to the first miss signal;

a first register which outputs the program address as a request address;

a second register which sets a first received program address as a start address in response to the interrupt signal;

a third register which generates the prefetch address using the start address;

a first subtraction unit which subtracts the start address from the request address to output the read address;

a second subtraction unit which subtracts the start address from the prefetch address to output the write address;

a hit/miss determination unit which outputs one of a hit signal and a second miss signal depending on a determination result;

a counter which counts the number of times the hit signal is output, accumulates the count value and outputs the accumulated count value; and

a control signal generator which enables the running flag signal in response to the interrupt signal and disables the running flag signal, if the accumulated count value reaches the threshold value.

21. The cache memory device of claim 20, wherein

the determination result outputs the second miss signal when the read address is not within a given address range of the cache memory block or the second instruction corresponding to the read address is invalid,

the control signal generator outputs a given control signal in response to the second miss signal,

the second register resets the start address in response to the control signal, and

the third register generates the prefetch address using the start address, which has been reset in response to the control signal.

22. A method of controlling a cache memory device in a digital signal processor (DSP), comprising:

(a) first providing a first instruction from a first cache memory to a DSP core in response to a program address received from the DSP core;

(b) second providing at least one second instruction from a second cache memory to the DSP core in response to the program address based

on at least one of an output of a first miss signal from the first cache memory and an enabling of a running flag signal by the second cache memory;

(c) disabling the running flag signal and ceasing step (b) when a number of second instructions provided to the DSP core reaches a given value;

(d) third providing a third instruction from a third cache memory to the DSP core in response to the program address based on at least one the first miss signal output from the first cache memory and a disabling of the running flag signal by the second cache memory;

(e) enabling the running flag signal at the second cache memory when an interrupt signal is received thereto from the DSP core.

23. The method of claim 22, further comprising:

(f) iteratively repeating steps (a) through (e) until there are no further instruction requests received from the DSP core.

24. The method of claim 22, wherein step (b) includes:

(b1) generating a read address from a program address;

(b2) outputting a second miss signal and resetting a start address if the read address is not within a given address range or if the second instruction corresponding to the read address is invalid;

(b3) transmitting the reset start address to receive a second write instruction to be stored;

(b4) generating a write address based on the reset start address and storing a second write instruction;

(b5) outputting a hit signal and the second instruction if the read address is within a given address range or if the second instruction corresponding to the read address is valid;

(b6) counting the number of times the hit signal is output; and

(b7) iteratively repeating steps (b1) through (b6) until a count value of the counting in step (b6) reaches a given value.

25. A cache memory device for a digital signal processor (DSP) that is controlled in accordance with the method of claim 10.

26. A cache memory device for a digital signal processor (DSP) that is controlled in accordance with the method of claim 22.

APPENDIX B – EVIDENCE SUBMITTED UNDER CFR 1.130, 1.131 OR 1.132

None.

APPENDIX C – RELATED PROCEEDINGS

None.

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Please find below and/or attached an Office communication concerning this application or proceeding.

Notification of Non-Compliant Appeal Brief (37 CFR 41.37)	Application No. 10/759,270	Applicant(s) JANG, HO-RANG
	Examiner Jae U. Yu	Art Unit 2185

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The Appeal Brief filed on *01 November 2007* is defective for failure to comply with one or more provisions of 37 CFR 41.37.

To avoid dismissal of the appeal, applicant must file anamended brief or other appropriate correction (see MPEP 1205.03) within **ONE MONTH or THIRTY DAYS** from the mailing date of this Notification, whichever is longer. **EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136.**

1. ☐ The brief does not contain the items required under 37 CFR 41.37(c), or the items are not under the proper heading or in the proper order.

2. ☐ The brief does not contain a statement of the status of all claims, (e.g., rejected, allowed, withdrawn, objected to, canceled), or does not identify the appealed claims (37 CFR 41.37(c)(1)(iii)).

3. ☐ At least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment (37 CFR 41.37(c)(1)(iv)).

4. ☒ (a) The brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings, if any, by reference characters; and/or (b) the brief fails to: (1) identify, for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function under 35 U.S.C. 112, sixth paragraph, and/or (2) set forth the structure, material, or acts described in the specification as corresponding to each claimed function with reference to the specification by page and line number, and to the drawings, if any, by reference characters (37 CFR 41.37(c)(1)(v)).

5. ☐ The brief does not contain a concise statement of each ground of rejection presented for review (37 CFR 41.37(c)(1)(vi))

6. ☐ The brief does not present an argument under a separate heading for each ground of rejection on appeal (37 CFR 41.37(c)(1)(vii)).

7. ☐ The brief does not contain a correct copy of the appealed claims as an appendix thereto (37 CFR 41.37(c)(1)(viii)).

8. ☐ The brief does not contain copies of the evidence submitted under 37 CFR 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner **and relied upon by appellant in the appeal**, along with a statement setting forth where in the record that evidence was entered by the examiner, as an appendix thereto (37 CFR 41.37(c)(1)(ix)).

9. ☐ The brief does not contain copies of the decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief as an appendix thereto (37 CFR 41.37(c)(1)(x)).

10. ☐ Other (including any explanation in support of the above items):

The appellant refers to the specification by paragraph number. The specification should be refered by page and line number.

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